Recently, development of so-called electronic still cameras, which are electronic imaging apparatuses capable of inputting image data to multi-media systems, is in force. The electronic still camera usually uses a solid-state imaging unit, such as a CCD imaging device, for obtaining images. The image obtained in such a camera is displayed on a liquid crystal panel of like view-finder, and can also be recorded in a recording medium in response to the depression of a trigger by the user. It has been demanded to further improve the image quality and operation control property of the electronic camera. To meet these demands it is indispensable to use a CCD imaging device having a large number of pixels and also that it is desirable to real time confirm image of the same view angle as picked-up image with a view-finder.

Replace the paragraph starting at page 2, line 15 with:

Fig. 6 shows a construction which is conceivable in the case where the interlace system is applied to the usual inter-line type CCD imaging device. This example is of four-phase drive type with a least recurrence unit of two pixels. For the sake of the brevity, 16 pixels are shown as a set. These sets of pixels are arranged successively one after another in the vertical direction of vertical transfer path. In the Figure, reference numerals 1 to 16 within rectangles each designate each pixel 1. A vertical transfer path 2 has two groups a and b of vertical transfer electrodes 1a, 1b to 16a, 16b. Two like sequence transfer electrodes in the two electrode groups are provided for each of the pixels in each set. Each pixel 1

is connected via a shift gate 3 to each transfer channel in the vertical transfer path 2 corresponding to each of the transfer electrodes 1a to 16a in the electrode group a. The vertical transfer electrodes are connected to corresponding ones of four shift pulse application lead lines 4, via which 4-phase shift pulses out of phase by 1/4 cycle with one another are applied. The 4-phase transfer pulses are successively applied to the transfer electrodes, which are grouped in groups each of four transfer electrodes, whereby the charge read out via the shift gates to the vertical transfer path 2 are transferred in one direction. In Fig. 6, reference numeral 5 designates connection electrodes for connecting the lead lines 4 to an external circuit.

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Replace the paragraph starting at page 10, line 4 with:

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Referring to the Figure, reference numeral 11 designates a single plate color CCD imaging device, which photoelectrically converts light to an electric signal and has an electronic shutter function. A scene light flux can be inputted through a lens 12 and a stop-shutter mechanism 13 to the CCD imaging device 11. The output of the CCD imaging device 11 is subject to noise removal and amplification in a pre-processor 14, which includes a correlated double-sampling circuit and a pre-amplifier. An A/D converter 15 converts the output of the pre-processor 14, inputted as analog data, to digital data. A camera signal processor 16 processes the signal from the CCD imaging device 11 as image data. An AF/AE/AWB detector 17 includes an AF detector for generating AF data for focus

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control on the basis of the image signal from the CCD imaging device 11 prior to the intrinsic photography, an AE detector for generating AE data for exposure control and an AWB detector for generating an AWB data for white balance level setting. The AF, AE and AWB data from the AF/AE/AWB detector 17 are supplied through a CPU 18 to the lens 12, the stop/shutter mechanism 13 (via stop/shutter driver 29) and the camera signal processor 16, respectively.

Replace the paragraph starting at page 11, line 28 with:

Fig. 3 partly shows a single vertical pixel column and a vertical transfer path 2 corresponding thereto. Like the CCD imaging device shown in Fig. 6, this CCD imaging device has a plurality of pixel groups 1, which are each constituted by 16 pixels in successive vertical arrangement and are successively arranged vertically along a vertical transfer path 2. The vertical transfer path 2 has two groups a and b of transfer electrodes 1a, 1b to 16a, 16b. Two like sequence transfer electrodes in the two electrode groups a and b are provided for each of the pixels 1 in each set. Each pixel 1 is connected via a shift gate 3 to each transfer channel in the vertical transfer path 2 corresponding to each of the transfer electrodes 1a to 16a in the electrode group a in the vertical transfer path 2. To the transfer electrodes 1a to 16a of the electrode group a, independent shift/transfer pulse application lead lines 4A are connected to permit gate pulse application and also independent gate pulse application to the shift gates. The respective pixels of the same order in the successively arranged pixel groups